ROUTING ARCHITECTURE WITH HIGH SPEED I/O BYPASS PATH

Abstract of the Disclosure

[0069] Improved routing architectures including one or more high speed input/output (I/O) bypass paths are provided for use in, for example, programmable logic devices (PLDs) such as field programmable gate arrays (FPGAs). The output bypass paths add additional routing connections to the routing architecture, providing faster connections between the output of a logic element (LE) in the PLD and external circuitry. In one embodiment, an output bypass path is used for directly connecting the output of the LE to the input of an I/O multiplexer of an I/O block. In another embodiment, the output bypass path also bypasses the I/O multiplexer, providing a direct connection between the output of the LE and a bypass multiplexer of the I/O block. Also provided is an input bypass path which provides direct connections between an input buffer of the I/O block and an otherwise dangling conductor at the periphery of the PLD's routing architecture.